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A Novel PPFHB Bidirectional DC-DC Converter for Supercapacitor Application

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Abstract—This paper presents a novel bidirectional DC-DC converter for the supercapacitor application. In the proposed converter, push-pull forward with half bridge (PPFHB) voltage doubler structure is used to reduce the number of the power switches and get higher voltage gain. Based on phase-shift modulation scheme, all the switches can realize zero-voltage-switching (ZVS) turn-on and bidirectional power flow can be controlled with phase-shift angle. The operating principles of the converter are described in detail, ZVS conditions are discussed, parameters are designed, and the experimental results based on the prototype controlled by DSP are presented to verify the validity of the analysis and design.

Index Terms—DC-DC converter, bidirectional, ZVS

I. INTRODUCTION

Supercapacitors, or ultracapacitors, with high power density and low equivalent series resistance (ESR), have the advantages like higher efficiency, larger current charge and /or discharge capacity, long lifecycle and low heating losses. With these characteristics, supercapacitor is a good option to be used in the many power conversion systems, such as hybrid electric vehicle (HEV), uninterruptible power supply (UPS), distributed generation (DG) system to improve the dynamic performance and stability of the system [1]. But supercapacitors also have some undesirable features such as the low voltage rating, variable terminal voltage compared to batteries. So in recent years, it has become an important topic to design and control the bidirectional dc-dc converter, as interface circuit connecting the supercapacitors to these systems to boost the terminal voltage and realize the bidirectional power flow.

To control the power flow, while regulating DC bus voltage and charging or discharging the supercapacitors, the buck boost converter has been implemented in applications where voltage gain is not high because of the limited duty cycle. For the high voltage ratio and isolation applications, many different topologies with transformer coupled, bidirectional dc-dc converters have been proposed. In [2], a dual active full-bridge (DAB) converter was proposed. Its symmetric structure with phase-shift control scheme enables the bidirectional power flow and ZVS for all switches [3]-[5]. But without a large inductor in the topology the rms value of the current will be very high (under the condition of big difference between the input voltage and output voltage), which results in lower efficiency [6]. Some other topologies based on the current-voltage-fed structure are also proposed [7]-[10]. Active clamp

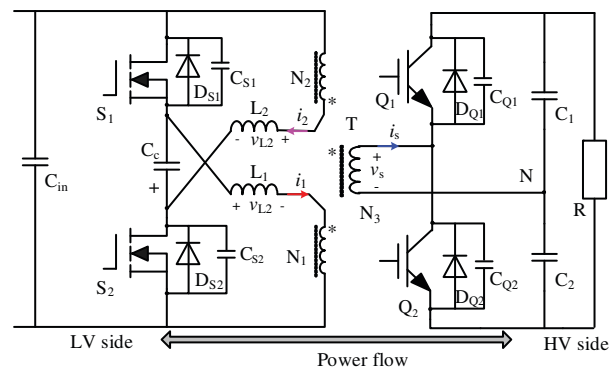


Figure 1: The topology of PPFHB bidirectional converter.

circuits or PWM plus phase-shift modulation schemes are used in these converters.

To increase the efficiency of DAB-type converter with wide-range variable input voltage caused by the supercapacitor, a novel bidirectional DC-DC converter is proposed in this paper, shown in Fig. 1.

The operation principle of the novel converter is discussed in section II, the characteristics of proposed converter are described in section III, and then some experimental results are shown in section IV. Based on the analysis, finally, conclusion is given in the last section.

II. ANALYSIS OF OPERATION

The proposed topology employs the push-pull-forward structure to reduce the number of the power switches. It can reduce the impedance of the current paths to lower the conduction loss caused by high rms current. the half-bridge voltage doubler circuit is utilized in the secondary side of the high frequency transformer to get high voltage transition ratio. The converter is controlled by the phase-shift (between the primary side and secondary side) technique for bidirectional power conversion. Because the voltage on the switches are always leading to the current, all the switches can operate under ZVS turn-on.

The principle of the proposed ZVS converter is explained using the idealized waveforms in Fig. 2. As the gate signal waveforms, the duty cycle is fixed at 50%. The switch pairs, S_1 , S_2 and Q_1 , Q_2 in the same half bridge, turn on/off complementarily with dead time. The the electrical angle reflected by the time difference between rising edge of S_1

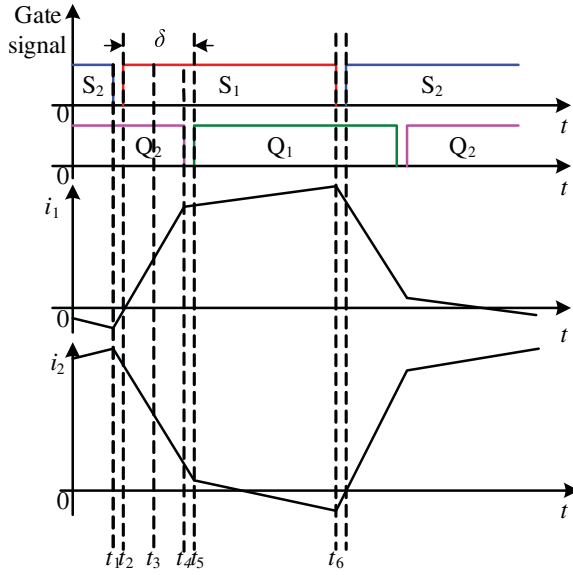


Figure 2: Switching waveforms of the converter.

and that of Q_1 is the phase shift to be used to control the output voltage of the converter and power flow direction.

To analyze the steady state operation, the followings are assumed:

- 1) All components and devices are ideal;
- 2) and large enough to be regarded as a constant voltage source;
- 3) The magnetizing current of the transformer could be ignored;
- 4) $L_1 = L_2 = L$, $C_{S1} = C_{S2}$, $C_{Q1} = C_{Q2}$.

Since the positive half cycle is similar to the negative half cycle except that the signs of voltage and current are reversed, the analysis here of the circuit operation is focused on the positive half cycle only.

Mode 1 ($0 \sim t_1$): The switches, S_2 and Q_2 are on-state on already, prior to t_0 and the primary currents of the transformer, i_1 and i_2 have the following current paths, respectively: $i_1 : V_{C_{c+}} \rightarrow S_2 \rightarrow N_1 \rightarrow L_1 \rightarrow V_{C_{c-}}$ and $i_2 : V_{in+} \rightarrow N_2 \rightarrow L_2 \rightarrow S_2 \rightarrow V_{in-}$. Base on the current paths, the circuit equations during this interval are described as:

$$\begin{aligned} nV_s - V_{Cc} &= L \cdot \frac{di_1}{dt} \\ V_{in} - nV_s &= L \cdot \frac{di_2}{dt} \end{aligned} \quad (1)$$

where V_{in} is the input voltage, the voltage on the supercapacitors; V_{Cc} is the voltage on the clamp capacitor, and in the steady state, $V_{Cc} = V_{in}$; V_s is the voltage on the secondary winding of transformer; n is the transformer turns ratio.

The power is transferred in the forward direction and the equivalent circuit of this mode is shown in Fig. 3 (a).

Mode 2 ($t_1 \sim t_2$): At t_1 , the switch S_2 is turned off and the energy stored in the L_1 and L_2 starts to charge C_{S1} and discharge C_{S2} at the same time. When the v_{CS2} reaches $2V_{in}$, the v_{CS1} equals to zero, D_{S1} turns on and the drain-source voltage of switch S_1 is clamped to zero approximately. At t_2 ,

S_1 turns on under ZVS. The current paths during this interval are shown in Fig. 3 (b).

Mode 3 ($t_2 \sim t_3$): S_1 remains on state. The i_1 increases and i_2 decreases with the same slope. The current paths are $i_1 : V_{in+} \rightarrow S_1 \rightarrow L_1 \rightarrow N_1 \rightarrow V_{in-}$ and $i_2 : V_{C_{c-}} \rightarrow D_{S1} \rightarrow N_2 \rightarrow L_2 \rightarrow V_{C_{c+}}$. The slope can be calculated by:

$$\begin{aligned} V_{in} + nV_s &= L \cdot \frac{di_1}{dt} \\ -V_{Cc} - nV_s &= L \cdot \frac{di_2}{dt} \end{aligned} \quad (2)$$

The equivalent circuit of this interval is shown in Fig. 3(c).

Mode 4 ($t_3 \sim t_4$): After t_3 , the value of i_1 is bigger than that of i_2 , so the current in the winding N_3 changes the direction converting to the switch Q_2 , but the voltage on the N_3 keeps negative clamped by C_2 . The equivalent circuit is shown in Fig. 3(d).

Mode 5 ($t_4 \sim t_6$): At t_4 , Q_2 turns off and it leads to charge and discharge the capacitors paralleled with Q_2 and Q_1 , respectively. When the voltage on the Q_2 increases to V_o , the antiparalleled diode D_{Q1} of Q_1 turns on and the voltage of N_3 changes direction immediately. The secondary side switches implement voltage conversion. At t_5 , Q_1 turns on under ZVS but because of the direction of the secondary current, i_s still goes through D_{Q1} until primary current conversion. The equivalent circuit of this interval is shown in Fig. 3(e). The circuit equations describing this stage are then given by:

$$\begin{aligned} V_{in} - nV_s &= L \cdot \frac{di_1}{dt} \\ -V_{Cc} + nV_s &= L \cdot \frac{di_2}{dt} \end{aligned} \quad (3)$$

Until the time t_6 , the converter begins the next half-cycle operation.

III. CHARACTERISTICS OF THE PPFHB CONVERTER

From the analysis in the last section based on operation principles, we can get some relationships among the parameters of the converter for the system design.

A. Output power

The delivered active power by this converter can be calculated, based on the waveform shown in Fig. 2, by:

$$P_o = \frac{N_1 \cdot V_{in} \cdot V_s}{N_3 \cdot \omega \cdot L} \cdot \frac{\delta \cdot (\pi - |\delta|)}{\pi}, \quad \left(-\frac{\pi}{2} \leq \delta \leq \frac{\pi}{2}\right) \quad (4)$$

with the limitation:

$$V_{in} \geq \frac{4P_o N_3 \omega L}{\pi N_1 V_s}, \quad \left(0 \leq \delta \leq \frac{\pi}{2}\right)$$

where ω is switching angular frequency (rad/s) of the PPF converter and HB converter and δ is phase shift angle (rad) which is defined to be positive when gate signal of S_1 is leading to that of Q_1 in phase.

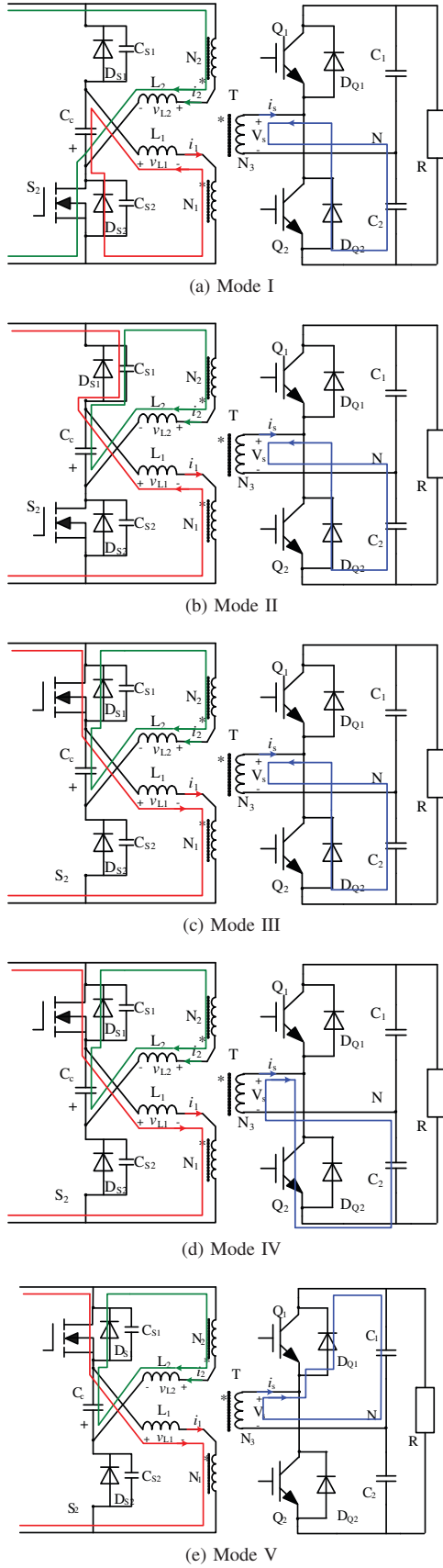


Figure 3: Circuit operations

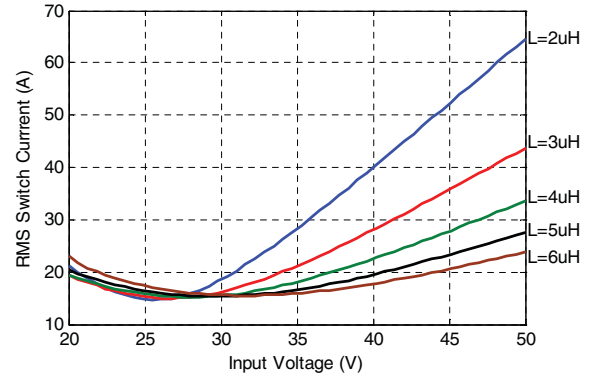


Figure 4: rms switch current curves with variable input voltage.

From the equation above, when the parameters of the system are constant, the active power is controlled by δ . When $\pi/2 \geq \delta \geq 0$, power will be delivered from the supercapacitor bank to the DC bus; and when $0 \geq \delta \geq -\pi/2$, DC bus will charge the supercapacitor bank so that the power direction will be reversed.

B. RMS values of the primary current

Based on the waveforms in Fig. 2, we can calculate the rms switch current in the primary side, I_1 and I_2 , as:

$$I_1 = I_2 = \sqrt{\frac{I_{P1}^2 + I_{P2}^2}{6} + \frac{I_{P1} \cdot I_{P2} (\pi - 2\delta)}{6\pi}} \quad (5)$$

where

$$I_{P1} = i_{1(t_4)} - i_{2(t_4)} = \frac{4nV_{in}\delta + \pi(V_o - 2nV_{in})}{4\omega nL}$$

and

$$I_{P2} = i_{2(t_1)} - i_{2(t_1)} = \frac{2V_o\delta + \pi(2nV_{in} - V_o)}{4\omega nL}$$

If the output voltage, V_o , is regulated very well, and with the parameters: $V_{in} = V_{SC} = 20 \sim 50$ VDC, $V_o = 200$ V, $P_o = 500$ W, $n = 4$, $\omega = 2\pi \cdot 40 \times 10^3$ rad/s, we can get the relationship between rms switch current and the variable input voltage, the voltage of the supercapacitor bank, shown in Fig. 4. Increasing the inductance L in the AC side can limit the rms current of the switch, but from equation (4) it also reduces the power delivery capability of the converter and bigger inductance will increase the reactive power requirement as well. On the other hand, the minimal rms current mostly depends on turns ratio of the transformer, and is located near the voltage $V_{in} = V_o/2n$. So based on the operating point, tradeoff between the parameters like L , n , can optimize the converter efficiency.

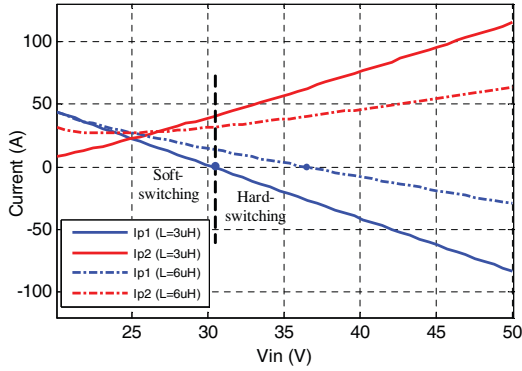


Figure 5: Relationship between value of I_{P1} , I_{P2} and ZVS operation.

C. ZVS conditions

In Fig. 1, the snubber capacitor is connected in parallel with each switch both to reduce switching loss and to damp out overvoltage. If the switch is turned on with its snubber capacitor discharged that means the antiparallel diode on, ZVS manner is to generate no or less switching loss. As described in Section II, the conversions for primary side switches and secondary side switches occur during interval $t_1 \sim t_2$ and interval $t_4 \sim t_5$, respectively. When both I_{P1} and I_{P2} are positive, every switch can turn on under ZVS, depending on the output power P_o , the phase shift δ , the input and output voltage, and the dead time. Under the same condition in the last subsection, the ZVS boundary is shown in Fig. 5. From Fig. 5 we can find that: when $V_{in} \leq V_o/2n$, $I_{P1} \geq I_{P2}$, and when $V_{in} > V_o/2n$, $I_{P1} < I_{P2}$ (also can get from equation (5)); and the hard-switching operation can only take place in the one side of transformer, whose voltage is lower than the other. At $V_{in} \simeq 30$ V, $I_{P1} \simeq 0$, and with V_{in} increasing the switches Q_1 and Q_2 lose the ZVS operation. At same time, increasing the inductance can extend the ZVS range, as the dashed lines shown in Fig. 5.

The minimum magnitude of I_{P1} or I_{P2} that can guarantee the ZVS operation is calculated as:

$$I_{min} = \sqrt{\frac{2V_{in}V_oC_s}{nL}} \quad (6)$$

where C_s is the capacitance of the paralleled snubber capacitor.

Based on the analysis above, achieving soft-switching operation becomes difficult with the wide-range variable input voltage, caused by the characteristics of the supercapacitors, and light load. But we can design different circuit parameters to choose switches in PPF converter or those in HB converter to operate under ZVS, according to the operating points and switching loss of different semiconductors used in different sides, to maximize the system efficiency.

D. Charging/discharging scheme

The schemes of supercapacitors charging can be divided into two categories: constant current charging and constant power

charging. The constant current charging is implemented by the DC-DC converter with constant current regulator. While constant power charging provides the fastest charge method that transfer all the available power from the charge source. In this paper, because of equation (4), the constant power charging method can be implemented easily.

At the starting stage of charging process, the voltage on the supercapacitors is about zero, and an inrush current flowing into the converter results in activating protection or system failure. The precharging operation described in [4] can be used in this converter. The PWM control is used in HB converter and the PPF converter works in synchronized rectifier mode with zero phase shift between the two sub-converters.

IV. EXPERIMENT

In order to verify the operation principle of the proposed converter, a prototype controlled by DSP was built in laboratory.

From the analysis above, the transformer and auxiliary inductors are important components to the converter performance. When supercapacitors bank outputs its lowest voltage, the low voltage side devices will have the maximum current stress, and the output power transferred through the transformer mainly depends on the auxiliary inductance, $L = L_1 = L_2$. According to this, the turns ratio of the transformer and auxiliary inductance should be designed to satisfy the following criteria: 1) at heaviest load condition, to keep the DC bus voltage constant, δ is limited under the maximum phase shift angle; 2) Trade-off between the turns ratio and auxiliary inductance is to lower rms current and extend ZVS operation range.

The one disadvantage of the PPF circuit is that the voltage stress on the MOSFET is doubled comparing with that in full-bridge circuit, so the high voltage MOSFET with higher on-state resistance, $R_{DS(on)}$, would be used leading to higher conduction loss. But in this application, the drain-source voltage of the MOSFET is at less than 200V, and nowadays, there are more and more very nice MOSFET commercial products with smaller $R_{DS(on)}$. So considering these characteristics, we can say that PPF structure is a reasonable choice. At the low voltage side, the peak current going through the switch is I_{P1} or I_{P2} , described as equation (5). At the high voltage side, the peak voltage for all the switches is the dc link voltage. The peak current of the voltage doubler is n times smaller than the low voltage side.

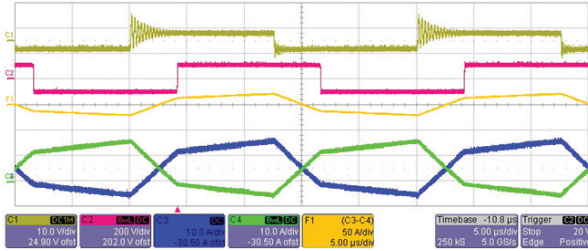
The specifications and parameters of the converter are given in Table I.

We can get the experimental results based on the prototype. From the waveforms shown in Fig. 6(a) with $\delta = 0.32\pi$ and Fig. 6(b) with $\delta = 0.4\pi$, under different input voltage, $V_{in} > V_o/2n$ and $V_{in} < V_o/2n$, respectively, the peak current points are changed from I_{P2} to I_{P1} . From Fig. 6(c), the secondary side current, i_S , has the same shape with that of $i_1 - i_2$, and the edges of v_S are decided by the falling edges of the gate-driving signals.

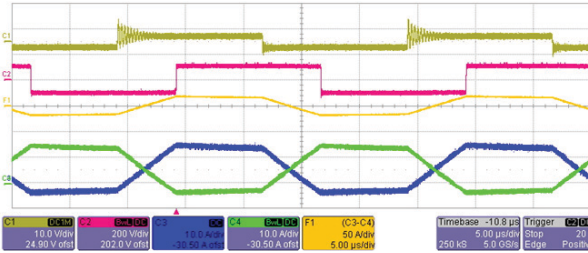
Devices switching waveforms with rated load are shown in Fig. 7. the swithes in both sides implemente ZVS-on. The

Table I: Parameters of the converter

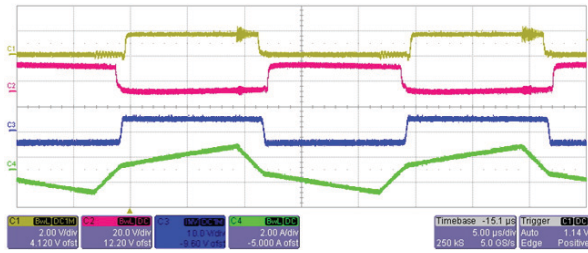
Input voltage in LV side	20 ~ 40 VDC
Output voltage in HV side	200 VDC
Rated power	500 W
Turns of the transformer	5 : 5 : 20
Transformer core material	N87
Auxiliary inductors	$L_1 = L_2 = 9 \mu\text{H}$
Inductor core material	N27
Capacitors	$C_1 = C_2 = 470\mu\text{F}/350\text{V}$ $C_{S1} = C_{S2} = 2200\text{pF}$ $C_e = 470\mu\text{F}/200\text{V}$
Switches S_1 and S_2	STW34NB20(200V/34A)
Switches Q_1 and Q_2	IRF450LC
Switching frequency	40 kHz
Digital controller	TMS320F2808



(a) CH1: voltage on the primary side (yellow one, 100 V/div); CH2: v_S (red one, 200 V/div); CH3: i_1 (blue one, 10 A/div); CH4: i_2 (green one, 10 A/div); F1: $i_1 - i_2$ (brown one, 50 A/div) when $V_{in} = 32$ V.



(b) CH1: voltage on the primary side (yellow one, 100 V/div); CH2: v_S (red one, 200 V/div); CH3: i_1 (blue one, 10 A/div); CH4: i_2 (green one, 10 A/div); F1: $i_1 - i_2$ (brown one, 50 A/div) when $V_{in} = 23$ V.



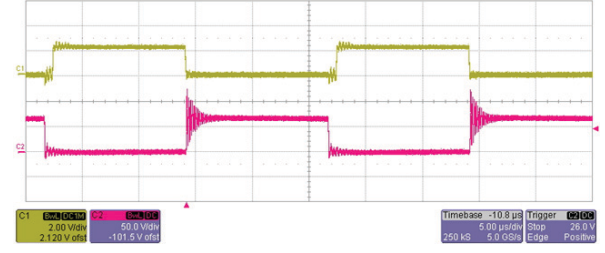
(c) CH1: voltage on gate-source of Q_1 (yellow one, 20 V/div); CH2: voltage on gate-source of Q_2 (red one, 20 V/div); CH3: v_S (blue one, 200 V/div); CH4: current i_S (green one, 2 A/div).

Figure 6: Waveforms of the PPFHB converter

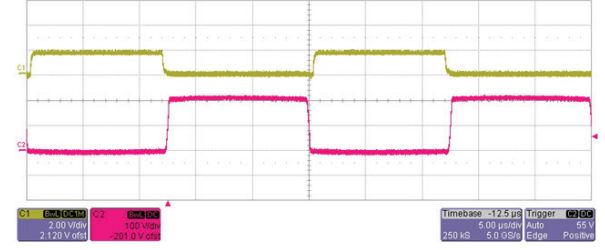
ringing on the drain-source voltage when it turns off, is caused by the parasitic components.

V. CONCLUSIONS

A novel ZVS bidirectional dc-dc converter with phase-shift control is proposed in this paper, which has the following advantages:



(a) Switch S_1 turns on under ZVS, CH1: voltage on gate-source of S_1 (yellow one, 20 V/div), CH2: voltage on drain-source of S_1 (50 V/div).



(b) Switch Q_1 turns on under ZVS, CH1: voltage on gate-source of Q_1 (yellow one, 20 V/div), CH2: voltage on drain-source of Q_1 (200 V/div).

Figure 7: Devices switching waveforms with rated load.

- 1) Reduce the number of the power switches in the high current side.
- 2) All switches realize ZVS.
- 3) Control scheme is simple and can implement bidirectional energy conversion flexibly.

These merits make that this kind of converter suitable for supercapacitors application in UPS system and EV system. Further work about modeling and control issue of the system will be published in the future.

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